Challenge Oriented Methodology for Analog Integrated Circuit Layout Design Training

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***Abstract*— This paper presents the course of Electronic Design offered by Tecnun (University of Navarra) in the Electronic Communication Engineering degree. The aim of this course is to bring the student closer to the professional integrated circuit layout world and it is oriented towards a final design challenge in which the students compete between them to obtain the maximum grade. Five modules with theory and lab work and the final project or challenge compose the course. Each module is focused on a certain component fabrication and solves a specific layout issue in the theory section. On the other hand, the practical work gains complexity progressively so the students can face the final challenge with guarantees. Once the challenge is completed, each student must present the design flow and the obtained results to the rest of the class and to a special panel of professional designers. During these presentations, the designs are evaluated from an industrial point of view. The implementation of this methodology has demonstrated that challenge orientated training improves the students interest in the course, their technical communication skills and prepares them for professional analog design scenarios.**

Keywords—Cadence, Layout, CMOS, Educational, IC.

I. INTRODUCTION

It is widely accepted nowadays that the key to the success of an engineering training program is the balanced combination of theoretical and practical courses. The instructor must provide the appropriate theoretical background to fully understand the physical processes involved in each subject, as well as developing the analytical tools and methods needed to apply that knowledge to solve real problems. Obviously, the objective of the practical courses should be the application of the concepts previously introduced to real case situations. However, on many occasions it is extremely difficult to reproduce a true industrial environment inside the walls of a lecturing room.

In the specific case of electronic circuit design, CAD tools offer new possibilities for training courses and practical application of theoretical knowledge. In addition, the use of professional electronic CAD tools may be also an objective per se in the curriculum of the students as it is a highly demanded skill.

Some years ago CAD required expensive workstations and computer networks but today a simple network of PCs with Linux as OS is powerful enough to run last generation professional tools and approach them to the students.

Taking advantage of this situation, 12 year ago an electronic design laboratory was set in Tecnun in order to train the students in professional electronic CAD tool use in parallel with the theoretical teaching of electronics. This program has been very successful during these years leading to the training of thousands of students. Because of that, in the new academic scenario defined by Bologna reform the importance of CAD in electronic courses has been not only maintained but also increased. Specifically, Table I presents the content of the subjects related with electronic design in the Electronic Communication Engineering degree of Tecnun.

TABLE I. SUBJECTS RELATED WITH ELECTRONIC DESIGN IN THE ELECTRONIC COMMUNICATION ENGINEERING DEGREE.

Year	*Subject*	*Theoretical content*	*Practical content*
1	Physics	Physical behaviour of semiconductors	-----
2	Electronic Technology	Semiconductors and basic amplifiers	-----
	Electronic Circuits	Basic circuits: Advances Amplifiers, Current sources.	Multisim
3	Electronic Design methods	Design methodology	Cadence simulation tool
	Radiofrequency	Analysis of the architectures of different communication systems.	ADS
	Electronic Communication	Design and characterization of RF modules: Mixers, LNAs, Oscillators…	Advanced design with Cadence simulation tool
4	Electronic Design	CMOS fabrication process	Cadence Layout tool

This paper is dedicated to the teaching methodology used in the Electronic Design subject of the 4º year of the degree. The theoretical content of this subject is devoted to CMOS technologies and integrated circuit implementation. These concepts are reinforced with the use of a professional integrated circuit (IC) layout tool during the course. Specifically, the students learn how to use the Layout XL tool of the Cadence environment, which is the industry standard for analog integrated circuit layout. As the students already have learn how to design and simulate integrated circuits in Cadence environment in previous subjects, after finishing the layout tool training they are able to complete all the steps of an IC implementation flow before sending it to its fabrication in the foundry (Fig. 1).

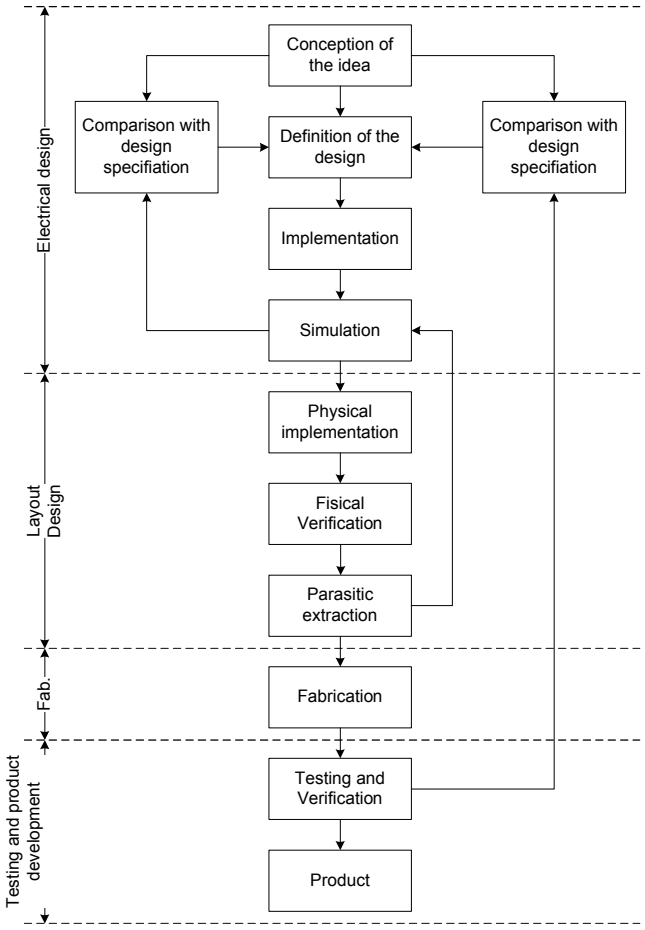

Fig. 1 Design flow an analog IC.

In addition to the content of the subject, this paper also presents its evaluation method, which is based on a competition based final project.

The structure of the paper is the following. In Section 2, course objectives are described. Next section is dedicated to the explanation of the course content module by module. Section 4 shows the evaluation method, in fact one of the innovations hereby presented. Next, conclusions are enunciated and last recommended bibliography is presented.

II. Course Objectives

The course has two main objectives. First goal is to train the students in the use of the most popular professional IC layout tools: Layout XL from Cadence environment. Second goal is to teach the students how the CMOS fabrication process is and how to reduce the effect of the fabrication process variations in the performance of a circuit using good layout techniques.

This learning is provided through the teacher's lessons and advices but also thanks to the comparison and kind competition with their classmates, as will be explained in the working methodology and evaluation sections.

In more detail, the intermediate objectives pursued by this course are:

- Learn the analog circuit design and fabrication flow, paying special attention to the layout phase.
- Learn the main dispersion sources in a CMOS fabrication process and their effect in the analog circuits.
- Learn what the mismatch and parasitic effects are in an IC and which are the most common techniques for their improvement at layout level.
- Train the students in the Cadence layout tool use.
- Learn how to interpret the design rules provided by the foundry in order to pass successfully the Design Rule Check (DRC) tool.
- Learn how to verify the circuit layout by using the Layout Versus Schematic (LVS) tool.
- Give the students the necessary tools to explain and justify a layout implementation in reports and in oral presentations using English.

Moreover, this course tries to change the mindset of its attendees; they have to change how they face problems. Up to this point, they have worked following the, let's say, classical academic problem-solution flow. But in a true working environment, is necessary to view things not as a problem but as goals to achieve. These goals are usually handed as specifications and design rules. Specifically in the layout of an IC they can be as diverse as the size of the circuit, number of allowable layers, parasitic effect of the layout or circuit symmetry. These design goals don't determine the layout and many solutions are possible for the same problem, being necessary detailed planning, good design techniques and lot of experience in order to optimize the circuit and avoid layout repetitions and waste of time.

This learning objective can be achieved using an appropriate evaluation method, in which creativity, working group capabilities and other features are integrated as part of the final mark. In order to do so a challenge based evaluation method has been selected in the final project of the subject.

III. Course Content

Five modules with theory and lab work and the final project or challenge compose the course. Each module is focused on a certain component fabrication and solves a specific layout issue in the theory section. On the other hand, the practical work gains complexity progressively. This progressive workload permits to reduce the apparent complexity of dealing with circuits with several transistors and the building block concept is developed. This way, when the students face the final project they have the tools to reduce the proposed layout into blocks and plan the design process properly.

The content of each module is explained in more detail next:

A. Module 1

In the theory part of the first module the basic concepts of IC are reviewed paying special attention to the differences between digital and analog circuits and integrated and discrete circuits. The objective of this module is to make the students aware of the importance of analog integrated circuits in current world. This way, the students can contextualize properly the subject and face it with enough motivation.

In the practical task of the first module the students review their previous training in Cadence Shematic Editor and simulation environment as well as their design skill obtained in previous courses. This is done going through a guided exercise and following the first steps of the circuit design flow presented in Fig 1. As a result the students finish with a circuit designed and simulated at schematic level.

B. Module 2

Up to this point, in the different subjects all over the degree the students have considered mostly the electronic components as a symbol (Fig 2.a) with a mathematical model that describes their behavior. In some cases they have implemented a circuit in a discrete board but they don't know much about how the integrated components work or how they look when they are implemented in a layout (Fig 2.b). Therefore, the objectives of this module are to present the cross section and the different layer of CMOS technologies, to introduce CMOS fabrication techniques and to describe the operation principle of the different integrated components.

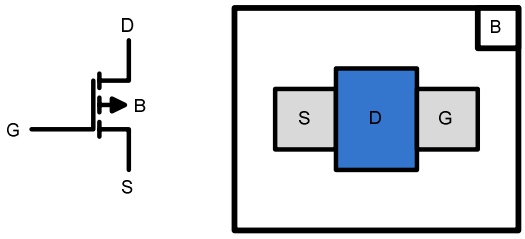

Fig. 2 a) Symbol representation of a NMOS transistor. b) NMOS transistor representation in a layout

In the practical task of this module the objective is to make the students familiar with the Layout XL design tool. In order to do that, the students have to finish a half-completed basic layout circuit. This way, they learn how to insert and modify components, connect blocks, resize metal path, generate guard rings, etc.

C. Module 3

In this module the different integrated capacitor models are introduced. The fabrication process of each model, their advantages and disadvantages and their main parameters are presented. In addition the concept of parasitic effect of connection paths is introduced to the students.

In the practical task the students will learn how to migrate a simple design with several capacitors from the schematic tool to the layout tool, prepare the layout, interconnect components them and use the different verification tools. Next, the students will extract the parasitic effects introduced by the connections and will generate a specific netlist called extracted view. This netlist will be afterwards characterizes and compared against the schematic at schematic netlist. Finally, the students will apply the techniques learned in the theory part to reduce the parasitic effects of the layout and approach the extracted view simulation results to the schematic simulation results.

D. Module 4

In this module the different integrated resistors models are introduced. The fabrication process of each model, their advantages and disadvantages and their main parameters are presented. In addition the mismatch effect, the common centroid technique and the dummies are presented to the students.

In the practical task the students will learn how to apply the common centroid technique in an implementation to reduce the mismatch effect in the circuit performance. In order to do so they will have to do the layout of two RC tanks with high symmetry requirements.

E. Module 5

In this module the different integrated CMOS transistors models are introduced. The fabrication process of each model, their advantages and disadvantages and their main parameters are presented. In addition some professional layout advices useful to face the final challenge are given to the students.

In the practical task the students will have to plan and do the layout of an astable oscillator composed by severals resistors and transistors. Before beginning the layout the students will have to present a report including a previous study and floor planning of the layout. This way the importance of the circuit planning is transmitted to the students

F. Final Project

The final project consists on the implementation, validation and simulation of a circuit. In order to do that, all the students are provided with the same schematic composed by a current source a current mirror and a LNA (Fig. 3).

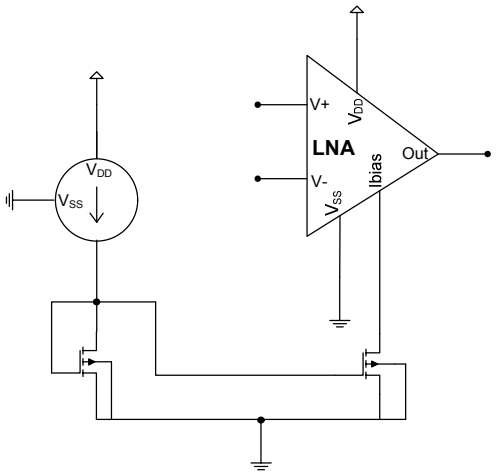

Fig. 3 Schematic of the final challenge

Together with the circuit schematic the student receive a Figure of Merit (FOM) that is afterwards used to evaluate the quality of the layout and rank the different implementation in the evaluation of this challenge. The FOM contains the size of the circuit, a factor related with the layout symmetry and a factor related with the circuit parasitic. The students will have a week to solve the circuits on their own and report all the design process. As the students will require tools from the Cadence design environment which are available only in the University facilities, they will compete between them at the same time in the same laboratory. This permits them comparing their work with their partners and increases their dedication and motivation to face the challenge. In addition they get used to work under pressure in a realistic scenario with real specifications and deadlines.

IV. Evaluation Method

According to the general objectives of the course, the evaluation of the work is carried out combining several exercises, in order to asses the progress of the students on different levels: Personal understanding of fundamentals, work capabilities and efficient time management. The use and understanding of English is taken for granted as they are future engineers.

Three main exercise categories are used to the evaluation: labs reports, challenge and final Exam. A maximum of 10 points can de awarded in total and the weight of each category is the following: 4 points correspond to the lab reports, 4 points correspond to the final challenge and 2 points correspond to the final exam.

A. Lab reports

After each practical case has been completed, students must fill a pre-defined form. The form has two parts: In the first one, questions cover the theoretical part of the work and the students are asked about theory and layout techniques. The second part is dedicated to the description of the layout. The aim of these questions is to provoke students to find the relation between theoretical and practical work, and also to learn how to report a layout to a superior in a realistic scenario. In addition, the continuous evaluation during the course gives a very useful feedback to the teacher about the subject evolution and the students understanding of it.

B. Final Challenge

As previously explained, in this exercise the students must face a real case design scenario of a relatively complex circuit, within a limited time frame (usually a weak). The same set of mandatory layout constraint is given to all the students and the circuit is evaluated in terms of the accomplishment of these requirements and some evaluations criteria, such as, the required area, the symmetry or the parasitic effects. Once the layout exercise is completed, each student must present his design flow and the obtained results to the rest of the class and to a special panel of designers. During these presentations, the designs are discussed, compared and ranked in terms of the FOM presented before the challenge. 2.5 point of the total score of the final challenge (4 point) are evaluated in terms of the presentation quality, planning, work execution, etc. However, the other 1.5 points of the grade are evaluated in terms of the FOM. Therefore, the student with the best FOM will obtain 1.5 point in the challenge part, whereas the student with the worst FOM will get a 0 in the challenge. The students in the between both will receive a ponderated amount of points depending on their position on the rank.

This method that may look a little bit aggressive has been also applied in other subjects with great results [8]. In both subjects the challenge oriented evaluation boosted the motivation of the students to face the subject especially during the final week. In addition, according to the students feedback, the final project evaluation under professional criteria and emulating a real scenario is a great opportunity to prepare their self for the real world.

C. Final Exam

At the end of the course, an individual exam is carried out. The objective of this exercise is to validate theoretical knowledge of CMOS fabrication techniques that may not be evaluated properly in the oral presentation of the challenge and lab reports.

V. Conclusions

It is widely accepted nowadays that the key to the success of an engineering training program is the balanced combination of theoretical and practical courses. Because of that in the degree of Electronic Communication Engineering of Tecnun University CAD tools are widely used to apply in the reality the theory and motivate students in the learning process. Specifically, in this article the course called Electronic Design is presented. The aim of this course is to bring the student closer to the professional integrated circuit layout world and it is oriented towards a final design challenge in which the students compete between them to obtain the maximum grade. Five modules with theory and lab work and the final project or challenge compose the course. Each module is focused on a certain component fabrication and solves a specific layout issue in the theory section. On the other hand, the practical work gains complexity progressively so the students can face the final challenge with guarantees

The inclusion of the competitive challege has proven to be an effective resource to improve students' interest in the course. Compared to the traditional exam, the challenges are powerful methods to increase the overall performance of the attendees. However, a special care must be taken into account in order to define a workload consistent with the time slot allocated for the test. The technical content of the exercise must be also adapted to the learning curve. If the design goals are too complicated, then students may get frustrated. Realistic goals within an appropriate time frame are the key to success.

Based on the comparison with previous years, the number of students not passing the final exam has been dramatically reduced. Polls conducted at the end of the term show a high level of satisfaction among participants.

Another educational tool proposed successfully at this course is the use of English as the official language. Most of the time it's the first time the students work in a foreign language, which is the "professional world language" and their interest and their efforts are constant and satisfactory.

The methodology introduced is also worthy for other engineering activities, and as a result of the experience and new skills learned, students effectively open their minds to new ways of solving problems.

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